Si4700/01/02/03 Programming Guide

1. Introduction

1.1. Scope

This document applies to Si4700/01/02/03 firmware revision 15 and greater and example code version 2 and greater. Refer to www.mysilabs.com for example code.

1.2. Purpose

The purpose of this programming guide is to describe the following:

- Device initialization sequence and busmode selection
- 2-wire and 3-wire busmodes
- Step-by-step procedures for
  - setting default configuration
  - channel selection
  - seek up/seek down
  - RDS/RBDS

This document references the Si4700/01 and Si4702/03 data sheets.

1.3. Terminology

SENB or $\overline{\text{SEN}}$—serial enable pin, active low, used only for 3-wire operation

SDIO—serial data in/data out pin.

SCLK—serial clock pin.

RSTB or $\overline{\text{RST}}$—reset pin, active low

Device—refers to the Si4700/01/02/03

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2. Hardware Description

2.1. Power, Initialization Sequence, and Busmode Selection

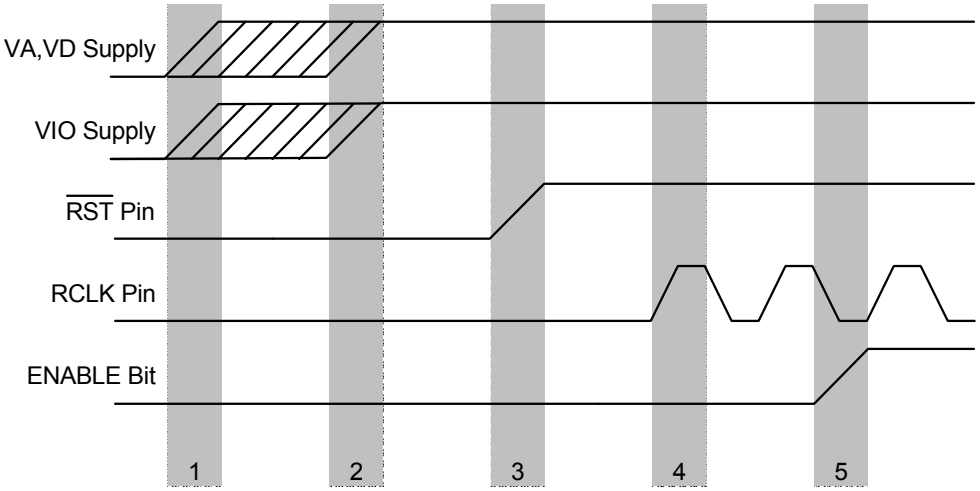


Figure 1. Initialization Sequence

2.1.1. Hardware Initialization

The FM tuner device is capable of communicating using either a 3-wire or 2-wire interface. The selection of this interface is made during the reset sequence.

Figure 1 demonstrates the sequencing of hardware events relative to reset. Figure 2 combines this information with the setting of the ENABLE and DISABLE bits to better describe the possible combinations. The following steps should be used to initialize the device properly.

1. Supply V_A and V_D.
2. Supply V_{IO} while keeping the RST pin low. Note that power supplies may be sequenced in any order (steps 1 and 2 may be reversed).
3. Configure the proper pins for bus mode selection. See Figure 3, “Powerup, Powerdown, and Reset Flowchart,” on page 7.
4. Set the RST pin high. The device registers may now be read and written.
5. Provide RCLK. If using the internal oscillator option, set the XOSCEN bit. Provide a sufficient delay before setting the ENABLE bit to ensure that the oscillator has stabilized. The delay will vary depending on the external oscillator circuit and the ESR of the crystal, and it should include margin to allow for device tolerances. The recommended minimum delay is no less than 500 ms. A similar delay may be necessary for some external oscillator circuits. Determine the necessary stabilization time for the clock source in the system.

   To experimentally measure the minimum oscillator stabilization time, adjust the delay time between setting the XOSCEN and ENABLE bits. After powerup, use the Set Property Command described in "5.1.Si4702/03 Commands (Si4702/03 Rev C or Later Device Only)" on page 31 to read property address 0x0700. If the delay exceeds the minimum oscillator stabilization time, the property value will read 0x1980 ±20%. If the property value is above this range, the delay time is too short. The selected delay time should include margin to allow for device tolerances.
6. Si4703-C19 Errata Solution 2: Set RDSD = 0x0000. Note that this is a writable register.
7. Set the ENABLE bit high and the DISABLE bit low to powerup the device.

   Unpredictable behavior could result if a non-zero value is present in the RDSD register of the Si4703-C19 when it is enabled. Note that no other device will experience this behavior. There are three solutions available to ensure a zero value in the RDSD register when the Si4703-C19 is enabled and only one solution need be selected.
   a. Solution 1—Generate a hard reset before enabling the tuner to clear the RDSD register. This is described in steps 2, 3, and 4 above and in step 1, To power up the device (after power down), of 2.1.2. "Hardware Powerdown” below. This must be done every time the tuner is enabled.
   b. Solution 2—Write a zero value to the RDSD register before enabling the tuner. This is described in step 6 above and must be done every time the tuner is enabled.
   c. Solution 3—Disable RDS by setting RDS = 0 before disabling the tuner. This is described in step 1, To power down the device, of 2.1.2. "Hardware Powerdown” below and must be done every time the tuner is disabled. When the device is disabled, the RDSD register is automatically set to zero in preparation for the next time the device is enabled.

2.1.2. Hardware Powerdown

A powerdown mode is available to reduce power consumption when the part is idle. Setting both the ENABLE bit high and the DISABLE bit high starts the powerdown sequence. This disables analog and digital circuitry while maintaining register configuration and keeping the bus active. Note that the device automatically sets the ENABLE bit low after the internal powerdown sequence completes. Setting the ENABLE bit low directly will cause the device to partially powerdown and should be avoided. See Figure 2. Setting the ENABLE bit high and the DISABLE bit low will bring the device out of powerdown mode and resume normal operation. Refer to Figure 1 for more information.

To power down the device:

1. Si4703-C19 Errata Option 3: Set RDS = 0.

2. Set the ENABLE bit high and the DISABLE bit high to place the device in powerdown mode. Note that all register states are maintained so long as V_{IO} is supplied and the RST pin is high.
3. Remove V_A and V_D supplies as needed.

To power up the device (after power down):

1. Si4703-C19 Errata Option 1: Perform a hard reset of the tuner by following steps 2, 3, and 4 of 2.1.1 Hardware Initialization.
2. Note that V_{IO} is still supplied in this scenario. If V_{IO} is not supplied, refer to device initialization procedure above.
3. Supply V_A and V_D.
4. Set the ENABLE bit high and the DISABLE bit low to powerup the device.

Setting the $\overline{RST}$ pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the $\overline{RST}$ pin high will bring the device out of reset, place the device in powerdown mode, and latch which bus mode will be used to communicate with the device. There are two methods for selecting the bus mode. Method one uses the $\overline{SEN}$ and SDIO pins while method two uses GPIO1 and GPIO3 (See Figure 3). Please refer to the data sheet for more information regarding bus selection and timing requirements of the RST signal.

More details on the register access during powerup and powerdown can be found in Section "3.2.1.ENABLE (02h.0)/DISABLE (02h.6)—Powerup Control" on page 11.

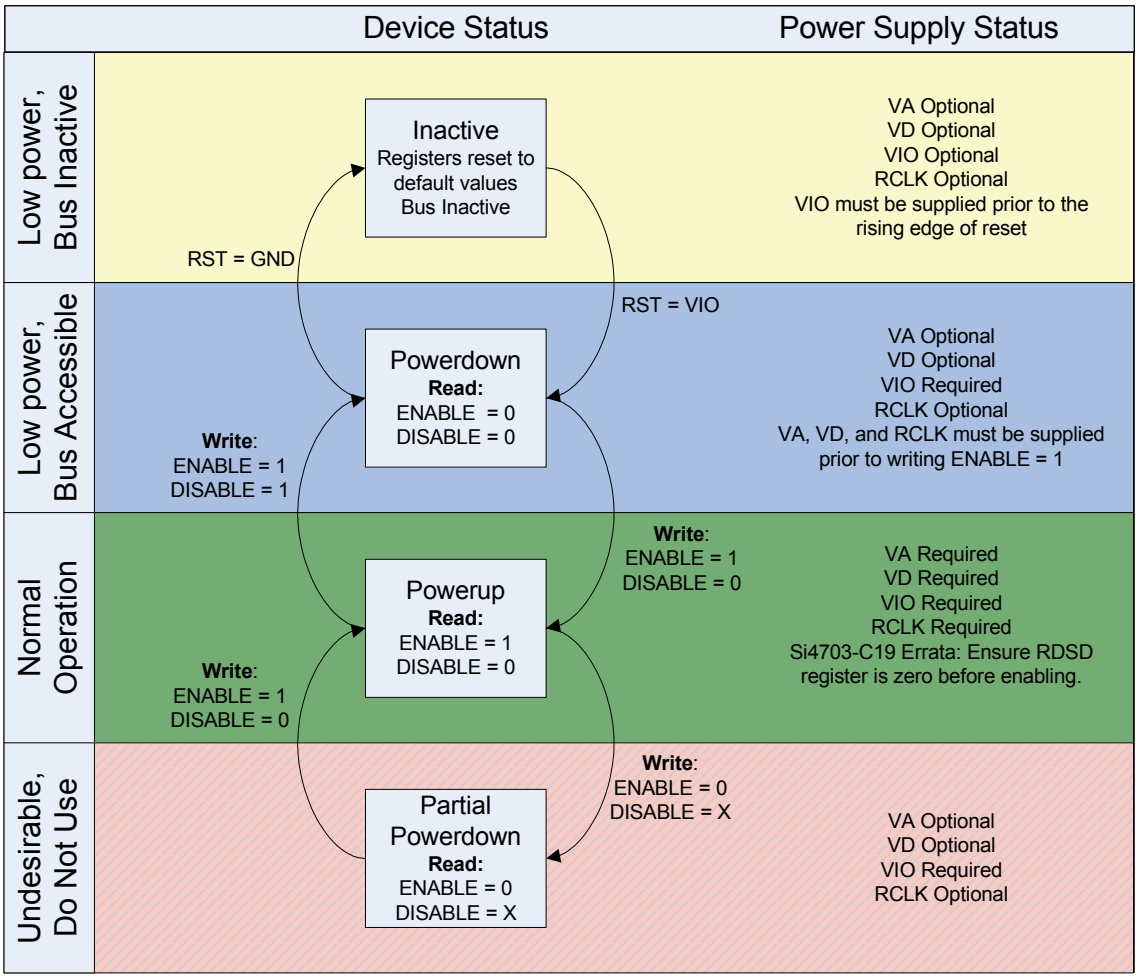
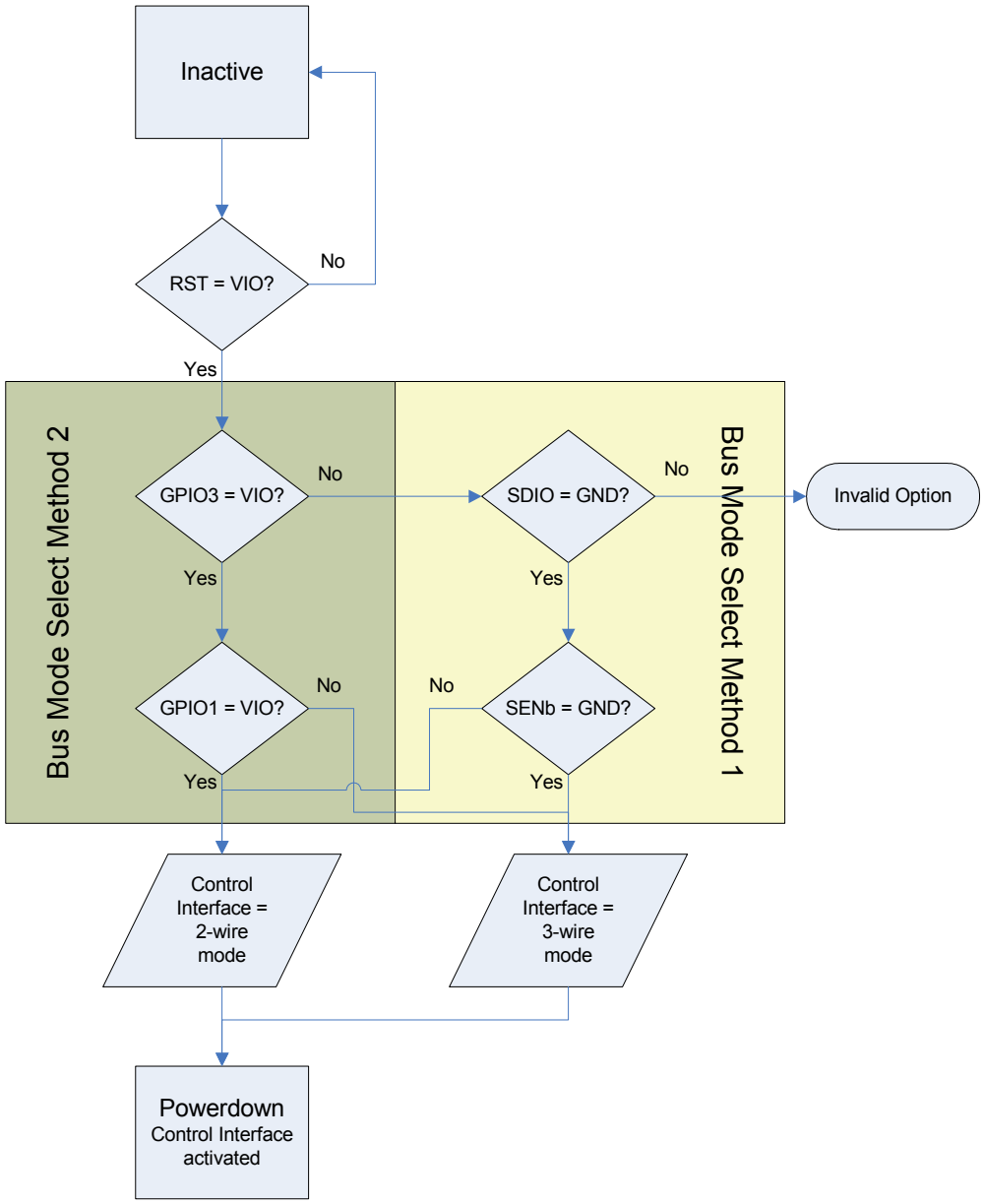


Figure 2. Powerup, Powerdown, and Reset State Diagram



Note: See data sheet for further details.

Figure 3. Powerup, Powerdown, and Reset Flowchart

2.2. 3-Wire Control Interface

For three-wire operation, a transfer begins when the SEN pin is set low on a rising SCLK edge. The control word is latched internally on rising SCLK edges and is nine bits in length, comprised of a four bit chip address A7:A4 = 0110b, a read/write bit (read = 1 and write = 0), and a four bit register address, A3:A0. The ordering of the control word is A7:A5, R/W, A4:A0, as shown in Figure 4.

For write operations, the serial control word is followed by a 16-bit data word and is latched internally on rising SCLK edges. The device does not latch the register write until the falling SCLK with SEN high.

Refer to “3-Wire Control Interface Characteristics” and “3-Wire Control Interface Write Timing Parameters” of the device data sheet for more information.

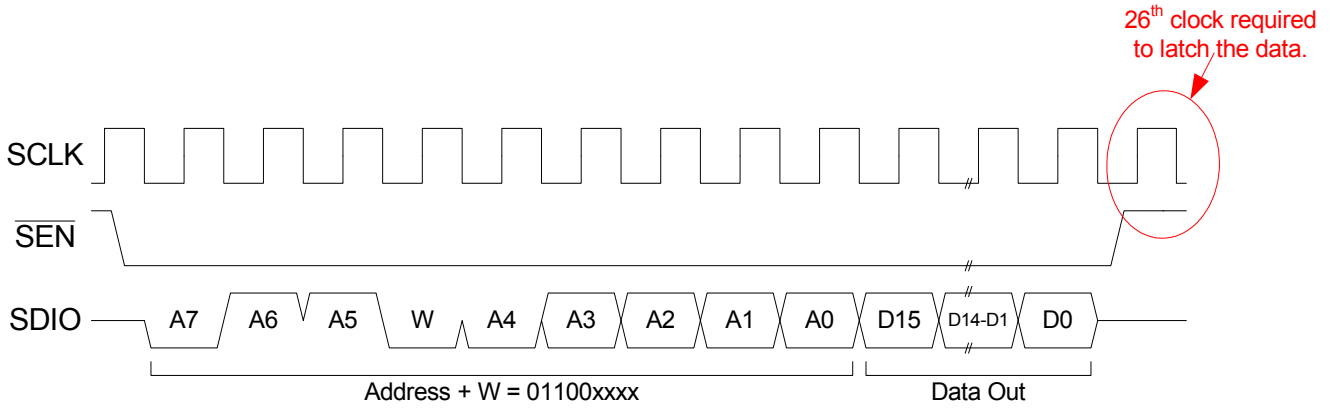


Figure 4. 3-Wire Control Interface Write Timing Diagram

For read operations, a bus turn-around of half a cycle is followed by a 16-bit data word shifted out on rising SCLK edges. The transfer ends on the rising SCLK edge after SEN is set high. Note that 26 SCLK cycles are required for a transfer; however, SCLK may run continuously.

Refer to “3-Wire Control Interface Characteristics” and “3-Wire Control Interface Read Timing Parameters” of the device data sheet for more information.

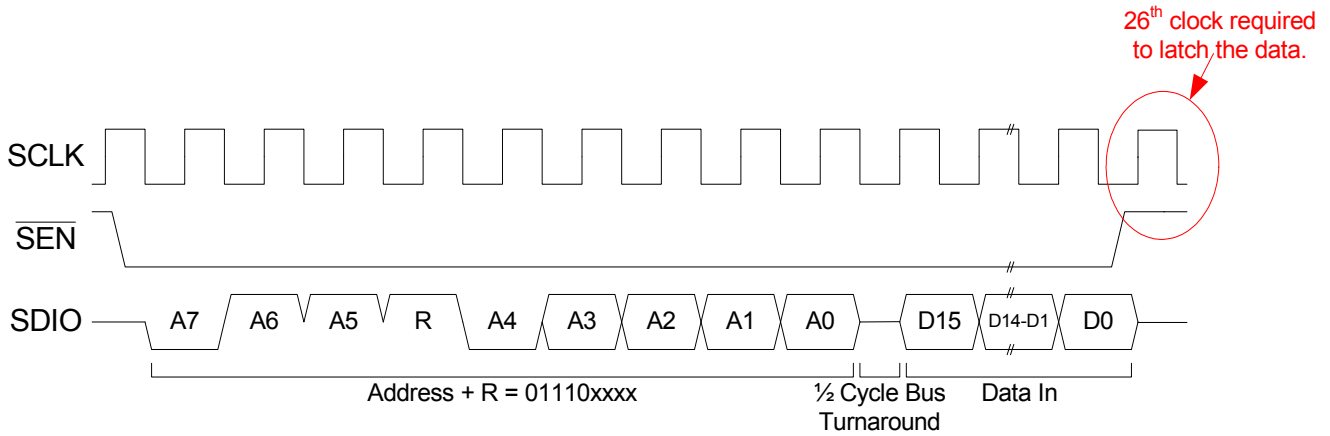


Figure 5. 3-Wire Control Interface Read Timing Diagram

2.3. 2-Wire Control Interface

For two-wire operation, a transfer begins with the START condition. A START condition is defined as a high to low transition on the SDIO pin while SCLK is high. Transitions for data bits must occur while the SCLK pin is low. The byte following the START is the control word. The control word is latched internally on rising SCLK edges and is eight bits in length, comprised of a seven bit device address equal to 0010000b and a read/write bit (read = 1 and write = 0). The ordering of the control word is A6:A0, R/$\overline{W}$ as shown below. The device remains in the read or write state until the STOP condition is received.

For write operations, the control word and device acknowledge is followed by an eight bit data word latched internally on rising edges of SCLK. The device always acknowledges the data by setting SDIO low on the next falling SCLK edge. Any number of data bytes may be written by repeating the write process without sending a STOP condition. Device register addresses are incremented by an internal address counter, starting with the upper byte of register 02h, followed by the lower byte of register 02h, and wrapping back to 00h at the end of the register file. The transfer is considered finished upon receipt of a STOP condition.

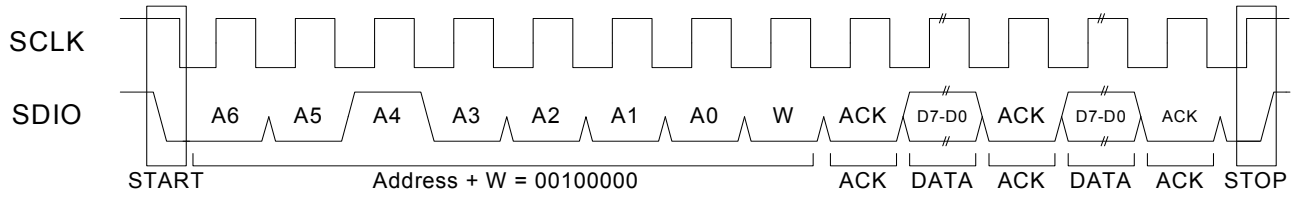


Figure 6. 2-Wire Control Interface Write Timing Diagram

For read operations, the control word and device acknowledge is followed by an eight bit data word shifted out on falling SCLK edges. Any number of data bytes can be read by sending a low ACK to the device. Device register addresses are incremented by an internal address counter, starting at the upper byte of register 0Ah, followed by the lower byte of register 0Ah, and wrapping back to 00h at the end of the register file. The transfer ends with the STOP conditions regardless of the state of the acknowledge.

Refer to “2-Wire Control Interface Characteristics” and “2-Wire Control Interface Read and Write Timing Parameters” of the device data sheet.

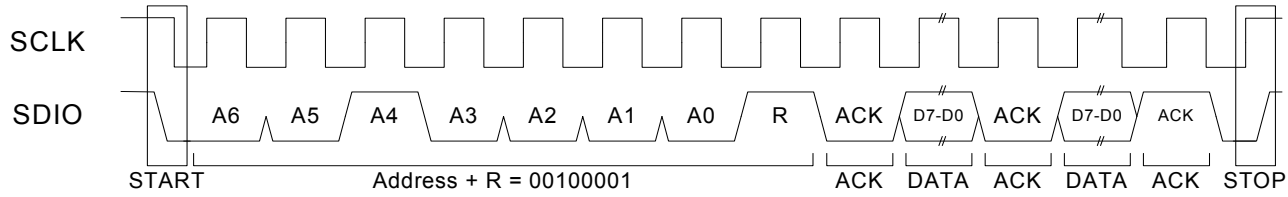


Figure 7. 2-Wire Control Interface Read Timing Diagram

3. Software Configuration

3.1. Registers

The control and status of the device is obtained through bitfields within 16 registers of 16 bits each. The functionality of the bits can be separated into two main categories: control and status. The control bits can be further subdivided into categories of when or how they are used (Table 1). While the status bits can be classified as static, static after power up, or dynamic after power up (Table 2).

Table 1. Register Use

Bit(s)	Hardware Control	General Config	Regional Config	End User Adjustable	Seek	Tune
DISABLE	X					
ENABLE	X					
XOSCEN	X					
AHIZEN	X					
GPIO1	X					
GPIO2	X					
GPIO3	X					
RDSIEN	X					
STCIEN	X					
BLNDADJ		X				
DSMUTE		X				
SMUTER		X				
SMUTEA		X				
VOLEXT		X				
SEEKTH		X				
SKSNR		X				
SKCNT		X				
RDSPRF		X				
RDSM		X				
RDS			X			
DE			X			
BAND			X			
SPACE			X			
DMUTE				X		
MONO				X		
VOLUME				X		
SEEKUP					X	
SKMODE					X	
SEEK					X	
TUNE						X
CHAN						X

Table 2. Status Bit Classification

Bit(s)	Static	Static After Power Up	Dynamic After Power Up
PN	X		
MFGID	X		
REV		X	
DEV		X	
FIRMWARE		X	
ST			X
RSSI			X
READCHAN			X
STC			X
SF/BL			X
AFCRL			X
RDSR			X
RDSS			X
BLERA			X
BLERB			X
BLERC			X
BLERD			X
RDSA			X
RDSB			X
RDSC			X
RDSD			X

3.2. Hardware Control Registers

The following set of registers alter the hardware in some way. These registers are typically the first group to be programmed.

3.2.1. ENABLE (02h.0)/DISABLE (02h.6)—Powerup Control

The ENABLE/DISABLE bits are analogous to the on/off buttons of the device. ENABLE=1 turns the device on while DISABLE=1 turns the device off (powerdown mode). When writing the register to place the device into powerdown mode, ENABLE should remain set to 1 while setting DISABLE to 1. The device clears the ENABLE and DISABLE bits, indicating the powerdown mode has been entered.

Table 3 shows the sequence of commands required to powerup the device. Note that address 07h may be written during powerup configuration.

Table 3. Powerup Configuration Sequence

Write address 07h (required for crystal oscillator operation). ■ Set the XOSCEN bit to power up the crystal. **Example:** Write data 8100h.
Wait for crystal to power up (required for crystal oscillator operation). ■ Provide a sufficient delay (minimum 500 ms) for the oscillator to stabilize. See 2.1.1. "Hardware Initialization" step 5.
Write address 02h (required). ■ Set the DMUTE bit to disable mute. Optionally mute can be disabled later when audio is needed. ■ Set the ENABLE bit high to set the powerup state. ■ Set the DISABLE bit low to set the powerup state. **Example:** Write data 4001h.
Wait for device powerup (required). ■ Refer to the Powerup Time specification in Table 7 "FM Characteristics" of the data sheet.
Read addresses 00h–01h (optional). ■ The bits PN[3:0] = 1 indicate the part family: Si4700/01/02/03. ■ The bits MFGID[11:0] = 242h indicate Silicon Laboratories as the manufacturer. ■ The bits REV[5:0] = 1 indicate silicon revision A. 2 indicates revision B. 3 indicates revision C. ■ The bit(s) DEV indicate the identity of the device. Firmware 16 changed the size of the DEV register from 1 bit to 4 bits and reduced FIRMWARE to 6 bits. Prior to firmware 16, DEV = 0 indicate the Si4700 and DEV = 1 indicate the Si4701 after powerup. For firmware 16 and later: DEV = 0000 after powerup = Si4700. DEV = 0001 after powerup = Si4702. DEV = 1000 after powerup = Si4701. DEV = 1001 after powerup = Si4703. ■ The FIRMWARE bits indicate the firmware revision after powerup.
Read addresses 02h-0Fh (optional) ■ Storing the values of each of the 16 registers locally is recommended to simplify manipulation of register bits and to reduce the number of reads/writes to the I/O bus. These are referred to as the shadow registers and can be stored in a 16 word array, `shadow_reg[]`. **Example:** To write bit 15 of register 07h after power up, write 07h as `shadow_reg[0x07] ^ 0x8000`
Write remaining hardware configuration registers (required). **Write the general configuration registers (required).** **Write the regional configuration registers (required).** These registers can be programmed in any order.

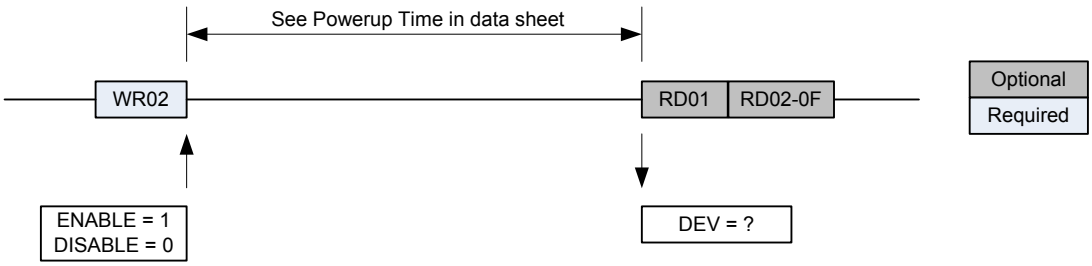


Figure 8. Powerup Timing

Table 4 shows the sequence of commands required to powerdown the device. As of Revision B, the tuner can optionally be programmed to place the audio output pins into a high impedance state. If this is desired, set the AHIZEN bit in register 07h prior to setting the disable bit. See "3.2.3.AHIZEN (07h.14)—Audio High-Z Enable" on page 13 for more information. To reduce powerdown mode current, GPIO1/2/3 can be programmed to output a digital low (GND). If this is desired, set the fields GPIO1-3[1:0] in register 04h to 10b prior to setting the disable bit. See sections 3.2.4 through 3.2.6 on page 14 and page 15 for more information.

Table 4. Powerdown Sequence

Write address 07h (optional for LOUT and ROUT Hi-Z). ■ Set AHIZEN. All other bits in this register should be maintained at the value last read (i.e., 0x3C04 or 0xBC04). **Example:** Write data 7C04h.
Write address 04h (optional for GPIO1/2/3 low). ■ Set GPIO1/2/3 to digital low to reduce current consumption. All other bits in this register should be maintained at the value last read. **Example**: Write data 002Ah.
Write address 02h (required). ■ Clear the DMUTE bit to enable mute. ■ Set the ENABLE bit high and DISABLE bit high to set the powerdown state. ■ After the DISABLE bit is set high, the device performs an internal powerdown sequence and then sets the ENABLE and DISABLE bits low. Setting the ENABLE bit directly to 0 will cause the device to partially powerdown. **Example:** Write data 0041h.

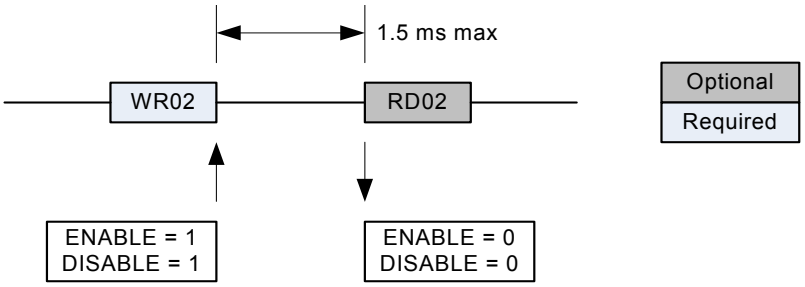


Figure 9. Powerdown Timing

3.2.2. XOSCEN (07h.15)—Crystal Oscillator Enable

Setting XOSCEN enables the internal oscillator. The internal oscillator requires an external 32.768 kHz crystal as shown in the data sheet schematic. If using this feature, the XOSCEN bit should be set at least 500 ms prior to setting the ENABLE bit and should be cleared only after setting the DISABLE bit. Unlike most bits, this feature will function regardless of the state of ENABLE/DISABLE. See 2.1.1. "Hardware Initialization" step 5 for timing details. When writing to this register the state of all other bits should be maintained. This can be accomplished by first reading the register to determine the state of the other bits. Alternatively, it is safe to assume that the value of bits 13:0 are 0x0100 prior to power up and are 0x3C04 after. This bit forces GPIO3 to become part of the oscillator circuit and it may not be used for anything else (i.e., stereo indicator). Because of this, bus mode selection method 1 must be used.

3.2.3. AHIZEN (07h.14)—Audio High-Z Enable

Setting AHIZEN maintains a dc bias of 0.5 x V_{IO} on the LOUT and ROUT pins. This prevents the device diodes from clamping to V_{IO} or GND in response to the output swing of other devices connected to these pins. With this bit set, multiple audio output devices can share a single input into an amplifier without the need for a multiplexer. Unlike most bits, this feature only functions while the device is in power down mode and V_{IO} is supplied. When writing to this register the state of all other bits should be maintained. This can be accomplished by first reading the register to determine the state of the other bits. Alternatively, it is safe to assume that the value of bits 13:0 are 0x0100 prior to power up and are 0x3C04 after.

3.2.4. GPIO1 (04h.1:0)—General Purpose I/O 1

GPIO1 can be programmed to 3 different states as shown in Table 5. This pin can be used to control an LED, another device in the system, or left unused.

Table 5. GPIO1 States

00	High impedance (default)
01	Reserved
10	Low output (GND level)
11	High output (V_{IO} level)

3.2.5. GPIO2 (04h.3:2)/RDSIEN (04h.15)/STCIEN (04h.14)—General Purpose I/O 2, Interrupts

GPIO2 can be programmed to 4 different states as shown in Table 6. When programmed as an interrupt, the Si470x device will generate interrupts based on the settings of RDSIEN and STCIEN. If RDSIEN is set a 5 ms interrupt pulse will be generated when RDS data is available. If STCIEN is set a 5 ms interrupt pulse will be generated upon completion of a SEEK or TUNE command. If both interrupts are enabled, the first interrupt after a SEEK or TUNE will be the STC interrupt. Subsequent interrupts will be RDS interrupts. This pin can also be used as a general purpose output or left unused. RDS is only available on the Si4701 and Si4703.

Table 6. GPIO2 States

00	High impedance (default)
01	STC/RDS interrupt
10	Low output (GND level)
11	High output (V_{IO} level)

3.2.6. GPIO3 (04h.5:4)—General Purpose I/O 3

GPIO3 can be programmed to 4 different states as shown in Table 7. When programmed as the mono/stereo indicator, the pin will reflect the status of the ST bit. When ST is set, indicating the tuner is in stereo mode, the pin will output a logic high. If the tuner switches into mono either because of poor SNR or a station that is not broadcasting in stereo, this pin will output a logic low. This pin can also be used as a general purpose output or left unused. Note that if the XOSCEN bit is set, GPIO3 is used for the crystal oscillator and this field is ignored.

Table 7. GPIO3 States

00	High impedance (default)
01	Mono/Stereo Indicator
10	Low output (GND level)
11	High output (V_{IO} level)

3.3. General Configuration Control Registers

The majority of the registers are set once at initialization and then left alone. These are provided to give the designer options and trade offs so the device can be tailored to a specific design.

3.3.1. BLNDADJ (04h.6:7)—Stereo/Mono Blend Level Adjustment

As the signal strength of a station diminishes, stereo noise can become overpowering. Switching to mono under these conditions removes the noise and allows even very weak stations to be heard clearly. To improve the listening experience, the device adjusts the amount of stereo separation based on the strength of the received RF signal. The point at which the device begins to blend stereo and mono signals can be selected from one of the 4 settings in Table 8. Figure 10 demonstrates the amount of stereo separation at a given RF level for each of the 4 settings. Where each of the lines in the graph meet 0 dB is the same point at which the stereo indicator bit, ST, toggles.

Table 8. BLNDADJ States

00	31–49 RSSI dBµV (default)
01	37–55 RSSI dBµV (+6 dB)
10	19–37 RSSI dBµV (–12 dB)
11	25–43 RSSI dBµV (–6 dB)

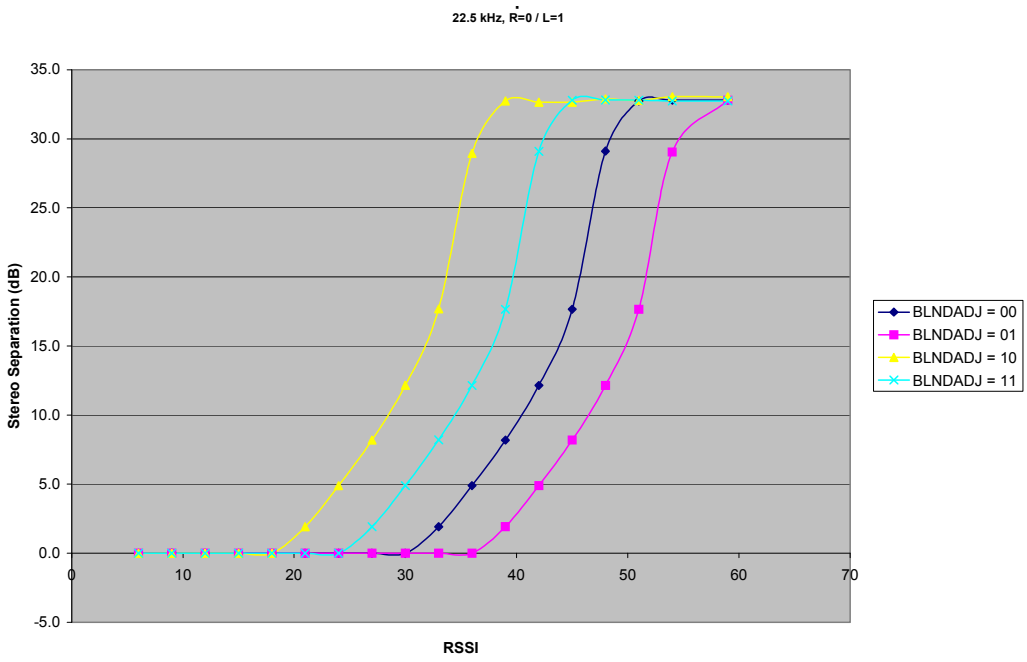


Figure 10. Stereo Separation

3.3.2. Softmute DSMUTE (02h.15)\SMUTER (06h.15:14)\SMUTEA (06h.13:12)—Disable Softmute\Softmute Attack/Recover Rate\Softmute Attenuation Level

To improve the listening experience when tuned to a non-existent station or one with poor SNR, the device provides a softmute feature which automatically reduces the volume significantly when the tuner detects that it isn't on a valid station. This feature can be disabled entirely by setting the DSMUTE bit. Additionally, this feature can be adjusted for how much it attenuates the volume (SMUTEA) as well as how quickly the attenuation is applied and removed (SMUTER). The available settings for SMUTEA and SMUTER are shown in the Tables 9 and 10 below.

Table 9. SMUTEA

00	16 dB
01	14 dB
10	12 dB
11	10 dB

Table 10. SMUTER

00	Fastest (default)
01	Fast
10	Slow
11	Slowest

3.3.3. VOLEXT (06h.8)—Extended Volume Range

By default, the VOLUME bits have a range of full scale (FS) down to FS-28 dB. Setting the VOLEXT bit shifts the range by 30 dB to be FS-30 dB down to FS-58 dB. This feature is only available in firmware 16 and later. This bit has been categorized as a general configuration bit rather than user adjustment because usually one of the two ranges is sufficient for volume adjustment. However, the usage of this bit is design dependent and depends greatly on what the LOUT and ROUT signals are being fed into. It can be used in conjunction with the VOLUME bits to adjust the input voltage into an audio amplifier.

Table 11. VOLEXT Settings

VOLEXT	VOLUME[3:0]	FW16 (dBFS)
1	0	Mute
1	1	–58
1	2	–56
1	3	–54
1	4	–52
1	5	–50
1	6	–48
1	7	–46
1	8	–44
1	9	–42
1	10	–40
1	11	–38
1	12	–36
1	13	–34
1	14	–32
1	15	–30

VOLEXT	VOLUME[3:0]	FW16 (dBFS)
0	0	Mute
0	1	–28
0	2	–26
0	3	–24
0	4	–22
0	5	–20
0	6	–18
0	7	–16
0	8	–14
0	9	–12
0	10	–10
0	11	–8
0	12	–6
0	13	–4
0	14	–2
0	15	0

3.3.4. SEEKTH (05h.15:8)—Seek RSSI Threshold

SEEKTH is the logarithmic Received Signal Strength Indicator (RSSI) threshold for the seek operation. RSSI is measured as the integrated power after the channel filter for a given channel. Channels with RSSI below the SEEKTH value will not be validated. Setting the seek threshold too high may result in missed valid channels; too low may result in false detections. SEEKTH is one of multiple parameters that can be used to validate channels. For more information and example settings, see "Appendix—Seek Adjustability and Settings" on page 35.

3.3.5. SKSNR (06h.7:4)—Seek SNR Threshold

SKSNR, the Signal to Noise Ratio threshold for the seek operation, compares a tuned channel's SNR to an SNR threshold to qualify the channel as valid. SKSNR is one of multiple parameters that can be used to validate channels. For more information and example settings, see "Appendix—Seek Adjustability and Settings" on page 35.

3.3.6. SKCNT (06h.3:0)—Seek Impulse Detection Threshold

FM Impulse noise occurs in all FM detectors when the SNR of a received station becomes very low and the received noise causes the FM detector to make instantaneous phase jumps, resulting in audible “clicks.” SKCNT sets the threshold for the number of FM impulses allowed on a tuned channel within a defined period. SKCNT is one of multiple parameters that can be used to validate channels. For more information and example settings, see "Appendix—Seek Adjustability and Settings" on page 35.

3.4. Regional Configuration Control Registers

While FM transmission is essentially the same around the world, there are a few differences between countries. This group of registers allows for customization to a given region.

3.4.1. BAND (05h.7:6)—FM Band Select

This register sets the range of tunable frequencies. The device supports 3 different ranges as shown in Table 12. The low limit of the range corresponds to what a CHAN of 0 represents. Depending on the SEEKUP setting, the high limit of the range is where the seek algorithm stops or wraps back around to the low limit.

Table 12. BAND Ranges

00	87.5–108 MHz (US / Europe, Default)
01	76–108 MHz (Japan wide band)
10	76–90 MHz (Japan)
11	Reserved (Do not use)

3.4.2. SPACE (05h.5:4)—FM Channel Spacing

The SPACE field defines the frequency steps that the least significant bit of the CHAN field represents. The device supports 3 different settings as shown in Table 13. This setting in conjunction with the BAND setting determines what frequency a given number in the CHAN register represents. See the description for CHAN for more information. The 50 kHz should only be used in those countries where transmission at 50 kHz spacing is allowed. For all other countries, the AFC will automatically correct for stations that are transmitting slightly off carrier. Selecting the proper spacing for the country the system will be used in will result in the best overall performance.

Table 13. SPACE Settings

00	200 kHz (US / Australia, Default)
01	100 kHz (Europe / Japan)
10	50 kHz
11	Reserved (Do not use)

3.4.3. DE (04h.11)—FM De-Emphasis

To reduce the amount of high frequency noise in an FM system, the transmitting station boosts (pre-emphasis) the high frequency content expecting that the receiving radio will reduce (de-emphasis) the high frequency content by the same amount. The amount is specified as the time constant of a simple RC filter. Two options are available: 75 µs (0), used in the USA; and 50 µs (1) used in Europe, Australia, and Japan.

3.4.4. RDS (04h.12)—RDS Enable (Si4701/Si4703 Only)

This bit enables/disables the RDS function of the device. When set high, RDS is enabled and when set low, RDS is disabled.

3.5. End User Adjustable Control Registers

Several register fields could be tied directly to an end user interface. Most designs will have an end user interface that gives access to some if not all of these features, but whether these features are implemented via the Si470x device or some other hardware in the design is system specific.

3.5.1. DMUTE (02h.14)—Disable Mute

Setting this bit high disables the mute feature. The audio output of the device can be muted in two ways; either by setting this bit low or by programming the VOLUME bits to 0.

3.5.2. MONO (02h.13)—Force Mono

Many end users find it desirable to force mono on stations with excessive stereo noise. While the device tries to avoid this situation with the stereo/mono blend feature, this bit provides the option to system designer. Setting MONO = 1 disables the stereo/mono blend feature and forces mono decoding of the FM baseband information regardless of signal SNR.

3.5.3. VOLUME (05h.3:0)—Volume

Volume is self explanatory. It adjusts the signal strength of the LOUT and ROUT pins. See the description of VOLEXT for the various settings relative to full scale output.

3.6. Seek Control Registers

One of the most powerful features of the device is the ability to automatically locate channels with valid content. Several registers control how seek behaves, however, this section is dedicated to those registers that could possibly change upon the execution of any seek operation.

3.6.1. SEEKUP (02h.9)—Seek Direction

The device has the ability to seek for stations in either direction. Setting this bit to 1 will cause the device to seek from the current channel up to the next available channel. Setting this bit to 0 will cause the device to seek down to the next available channel.

3.6.2. SKMODE (02h.10)—Seek Band Limit Behavior Mode

The device has the ability to stop seeking when a band limit (see BAND) is reached or to wrap around to the other end of the band. Setting this bit causes the former behavior, i.e. if seeking up and 108 MHz is reached, the device will stop seeking and set the SF/BL bit. Clearing this bit will cause the device to instead wrap back to 76 or 87.5 MHz depending on the setting of BAND. This bit qualifies as one that may be changed at seek time because of the various features the designer may want to provide to the end user. For example, a feature that scans the entire band for all valid stations is most likely to begin at CHAN = 00 and go to the end of the band. For that feature, SKMODE = 1 is the best choice. However, to provide a feature that seeks up or down from the currently tuned station, SKMODE = 0 is likely the better choice.

3.6.3. SEEK (02h.8)—Seek

This bit indicates that the device should begin a seek operation using the currently programmed seek settings (SKMODE, SEEKUP, SEEKTH, SKSNR, SKCNT). The operation can be aborted by clearing this bit, but this may leave the device on an invalid channel. During normal operation, the designer will leave this bit set until the device sets the STC bit. Once the STC bit is set, the designer should then clear the SEEK bit. Status of the seek operation can be obtained by polling the READCHAN register which is updated by the device as the SEEK progresses through the band. The following flow chart shows a typical seek algorithm.

Normally when SF/BL is set, the current channel is invalid. However, there are two exceptions. The first occurs when SKMODE = 0 and there is only one valid channel on the entire band. If the seek is started from that one valid channel, it will wrap the entire band and end on the valid channel it started from. Since the limit of the seek has been reached, the SF/BL bit will be set. The second exception occurs when SKMODE = 1 and there is a valid channel exactly at the band limit. Because the SEEK has hit the band limit, the bit will be set. To check for a valid station at the band limits, tune to the station just above the lower limit. Set the SKMODE = 0, SEEKUP = 0, and SEEK = 1. If there is a valid station at the limits, it will be detected.

Table 14 shows the sequence of commands required for seek and assumes that the Powerup Configuration, detailed in Section 2.1. "Power, Initialization Sequence, and Busmode Selection”, has completed. This table is intended to be used in conjunction with the seek flowchart in Figure 12.

Table 14. Seek Up/Seek Down Sequence

Write address 02h (required). ■ Set the SKMODE high to stop seek at the band limits and low to wrap at the band limits. ■ Set the SEEKUP bit high to seek up and low to seek down. ■ Set the SEEK bit high to begin the seek operation. ■ Keep all other bits at the previously configured setting. This is most easily done by maintaining an array of the settings. This array is referred to throughout this document and in the example code as si470x_shadow. **Example: SKMODE = 1:** `si470x_shadow[2] |= 0x0400` **SEEKUP = 0:** `si470x_shadow[2] &= ~0x0200` **SEEK = 1:** `si470x_shadow[2] |= 0x0100` `si470x_reg_write(2)`
Wait for GPIO2 = 0 (required for interrupt method). ■ This indicates that a seek/tune operation has completed.
Read address 0Ah (required). ■ The STC bit being set indicates tuning has completed. ■ The SF/BL bit being set indicates the seek operation searched the band without finding a channel meeting the seek criteria (SEEKTH, SKSNR, SKCNT). ■ The ST bit being set indicates stereo operation. ■ The bits RSS[7:0] indicate RSSI level for the current channel.
Read address 0Bh (optional). ■ The bits READCHAN[9:0] indicate the current channel. This can be read prior to STC = 1 if a seek progress indicator is desired.
Write address 02h (required). ■ Set the SEEK bit low to end the tuning operation and to set the STC bit low. **Example:** Write data to 4001h.
Read address 0Ah (optional). ■ The STC bit being cleared indicates that the TUNE or SEEK bits may be set again to start another tune or seek operation. Do not set the TUNE or SEEK bits until the Si470x clears the STC bit.

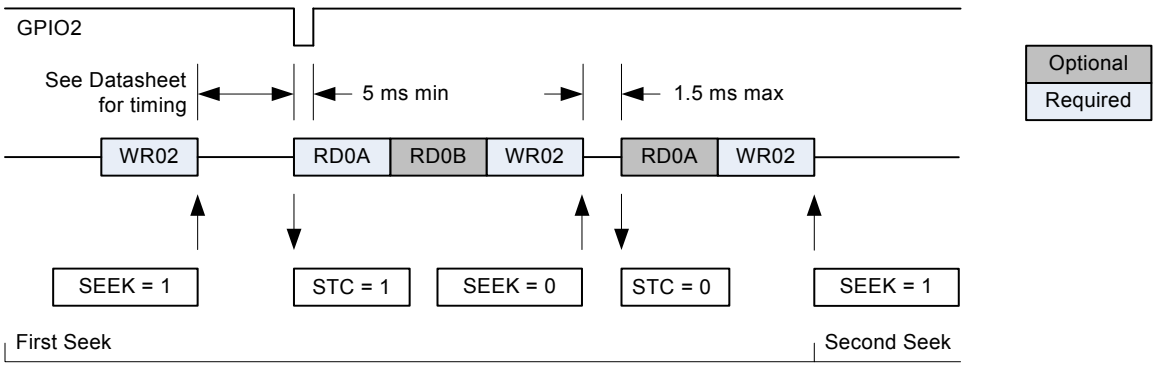


Figure 11. Seek Timing

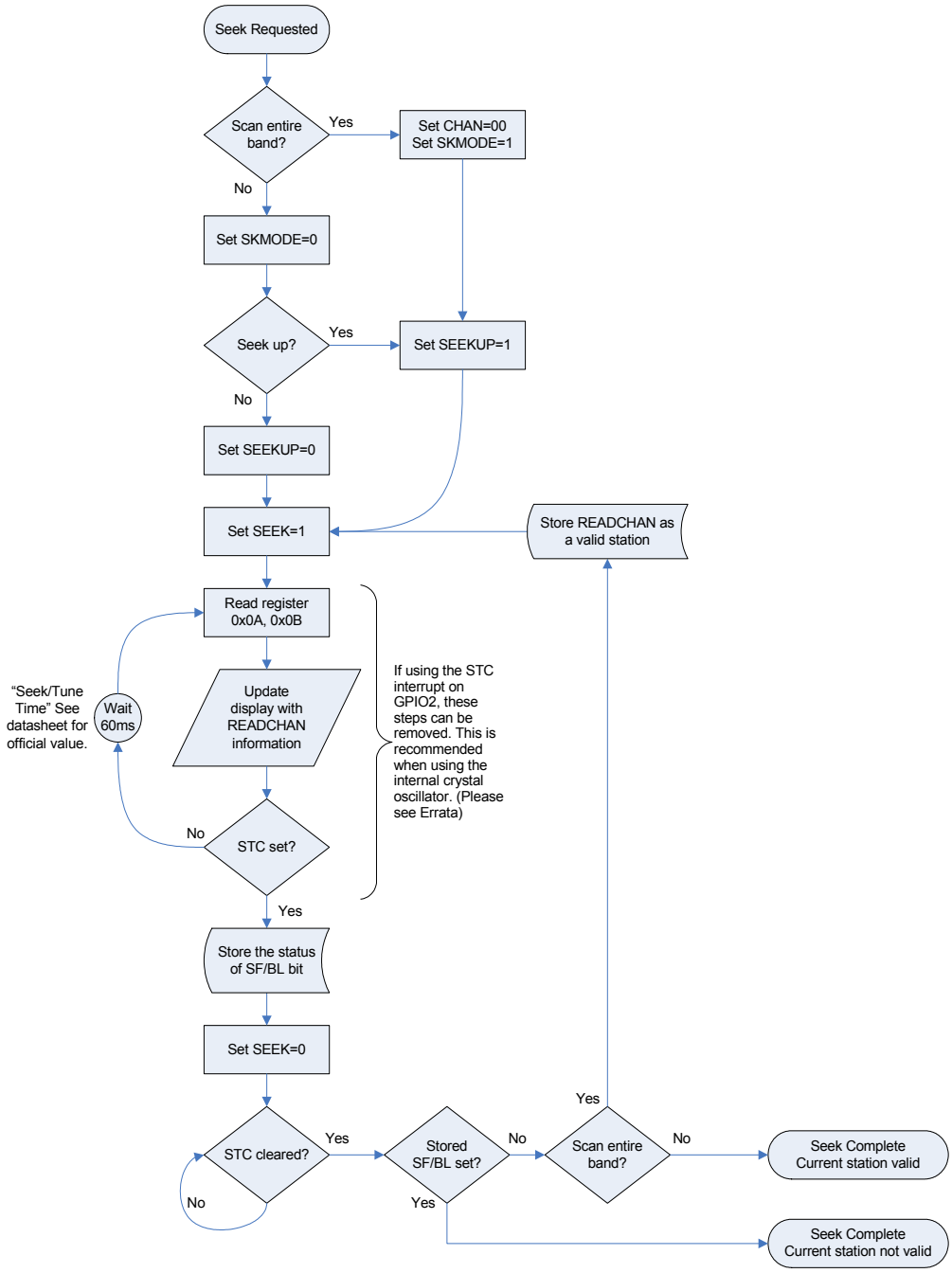


Figure 12. Seek Flowchart

3.7. Tune Control Registers

3.7.1. TUNE (03h.15)\CHAN (03h.9:0)—Tune\Channel Select

Setting the TUNE bit initiates the tuning process causing the device to switch to the frequency indicated by CHAN. The actual frequency that CHAN refers to depends on the BAND and SPACE settings and can be determined as follows:

Where:

- F is desired frequency in MHz
- S is space between channels in MHz (0.050, 0.100, or 0.200 MHz)
- C is integer channel setting
- L is minimum band limit in MHz as set by BAND (76 or 87.5 MHz)

F = S x C + L

As an example, if BAND = 00, SPACE = 01, and CHAN = 148, the frequency is 0.1 x 148 + 87.5 = 102.3 MHz

When the device completes the tuning process, the STC bit is set. The maximum time that the process takes is specified in the data sheet as "Seek/Tune Time". If GPIO2 is configured as an STC interrupt, the GPIO2 pin will pulse low for a minimum of 5ms. To clear the STC bit, clear the TUNE bit. It is important to verify that the STC bit is cleared before performing another seek or tune.

Table 15 shows the sequence of commands required for channel selection and assumes that the Powerup Configuration, detailed in Section 2.1. "Power, Initialization Sequence, and Busmode Selection", has completed.

Table 15. Channel Selection Sequence

Write address 03h (required). ■ Set the TUNE bit high to begin a tuning operation. ■ Set CHAN[9:0] bits to select the desired channel. **Example:** To tune to 103.5 MHz in the United States, with BAND[1:0] = 00 and SPACE[1:0] = 00 as described in the powerup sequence, set CHAN[9:0] = 80d = 50h such that frequency = 103.5 MHz = 0.200 MHz x 80 + 87.5 MHz). Write data 8050h.
Wait for GPIO2 = 0 (required for interrupt method). ■ This indicates that a seek/tune operation has completed.
Read address 0Ah (optional for interrupt method, required for polling method). ■ The STC bit being set indicates tuning has completed. ■ The ST bit being set indicates stereo operation. ■ The bits RSSI[7:0] indicate RSSI level for the current channel.
Read address 0Bh (optional). ■ The bits READCHAN[9:0] indicate the current channel.
Write address 03h (required). ■ Set the TUNE bit low to end the tuning operation and to set the STC bit low. **Example:** Write data to 0050h.
Read address 0Ah (optional). ■ The STC bit being cleared indicates that the TUNE or SEEK bits may be set again to start another tune or seek operation. Do not set the TUNE or SEEK bits until the Si470x clears the STC bit.

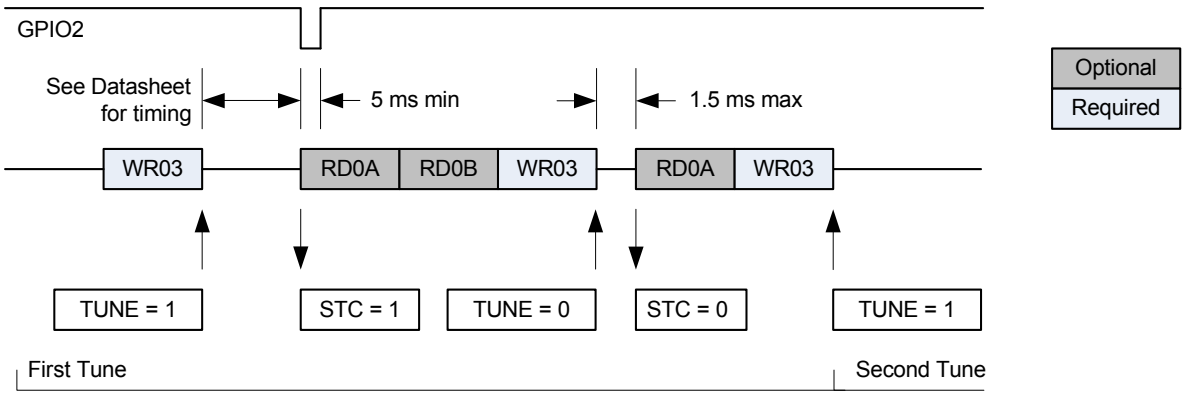


Figure 13. Channel Selection Timing

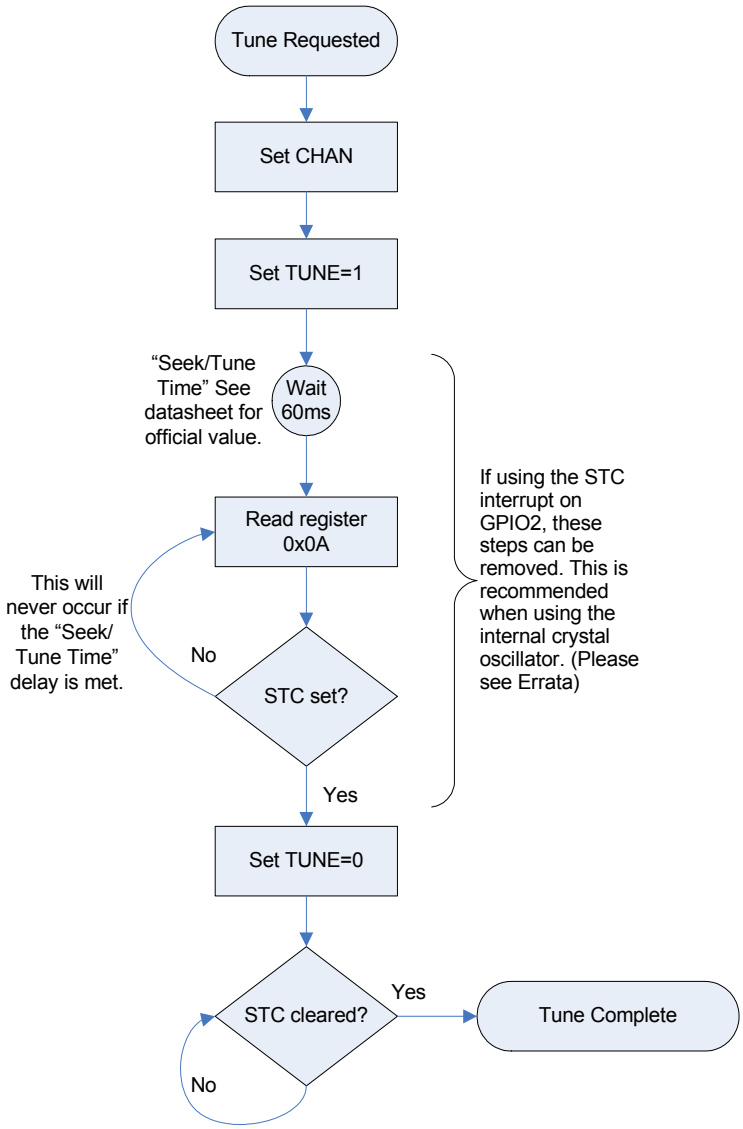


Figure 14. Channel Selection Flowchart

3.8. RDS/RBDS (Si4701/03 Only)

Table 16 shows the sequence of commands required for RDS and assumes that the powerup, initialization, and regular configuration has completed. The flow chart in Figure 16 should be used in conjunction with the example code found in rds.c. For more information on RDS, please refer to “AN243: Using RDS/RBDS with the Si4701/03".

Table 16. RDS/RBDS Sequence

Write address 02h (optional). ■ Select the RDS mode to use: standard or verbose. Standard mode only returns fully corrected data while Verbose mode indicates the number of errors corrected in each block.
Write address 04h (required for interrupt method). ■ Set the RDSIEN bit high to enable a low interrupt on GPIO2 when RDS data are ready. ■ Set the RDS enable bit (RDS = 1). ■ Set GPIO2[1:0] = 01 to enable STC and RDSR interrupts on GPIO2. **Example:** To enable RDS operation with RDS interrupts and seek/tune interrupts enabled, write data D004h.
Wait for GPIO2 = 0 (required for interrupt method). ■ This indicates that RDS data are ready.
Read address 0Ah (optional for interrupt method, required for polling method). ■ The RDSR bit being set indicates RDS data are ready (Si4701 only). ■ If in verbose mode, the BLERA bits indicate how many errors were corrected in block A. If BLERA indicates 6 or more errors, the data in RDSA should be discarded. ■ When using the polling method, it is best not to poll continuously. The data will appear in intervals of ~88 ms and the RDSR indicator will be available for at least 40 ms, so a polling rate of 40 ms or less should be sufficient.
Read address 0Bh (optional). ■ If in verbose mode, the BLERB, BLERC, and BLERD bits indicate how many errors were corrected in the respective blocks. If BLERB indicates 6 or more errors, all 3 blocks of data should be discarded. If BLERC or BLERD indicate 6 or more errors, then just the respective block may be discarded.
Read addresses 0Ch–0Fh (required). ■ The bits RDSA[15:0], RDSB[15:0], RDSC[15:0], and RDSD[15:0] contain error-corrected RDS group data.

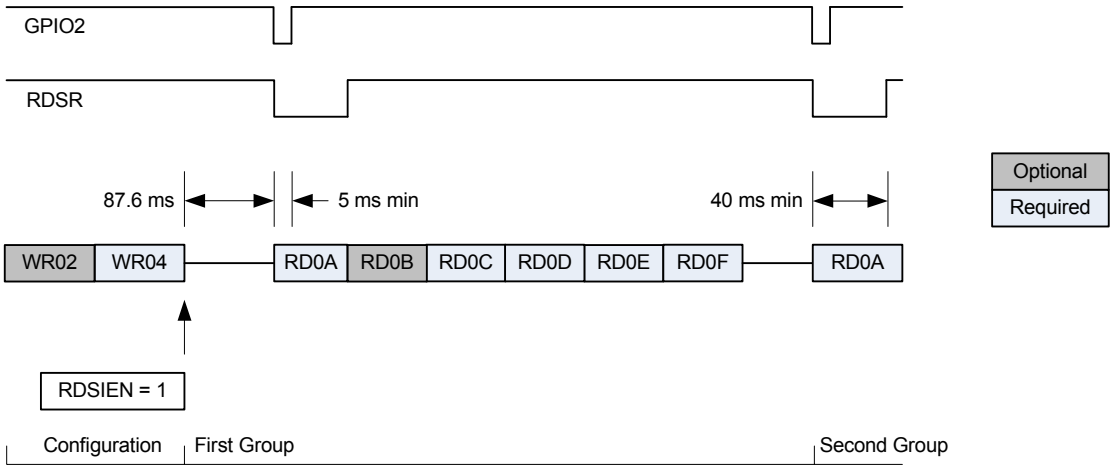


Figure 15. RDS Timing

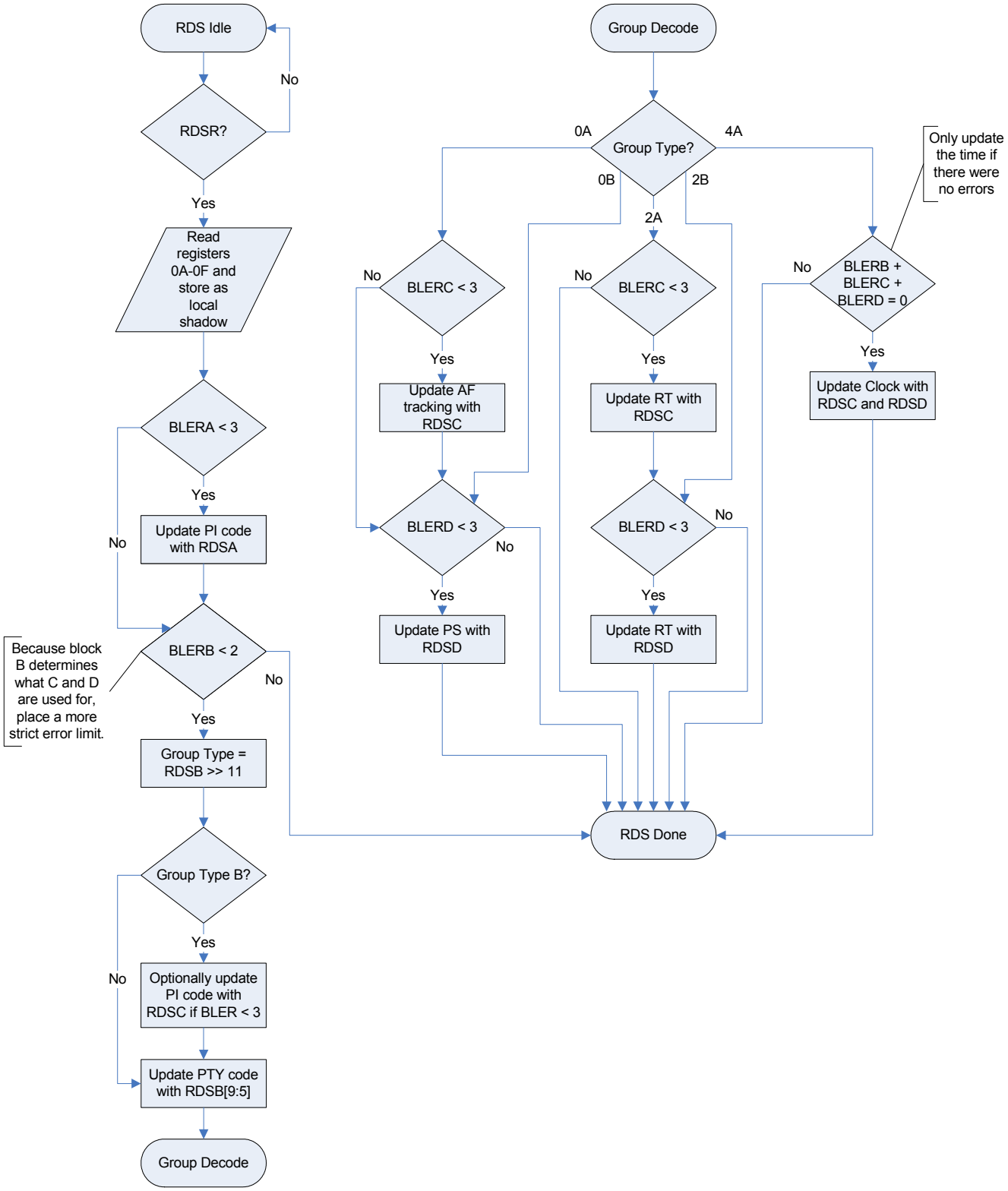


Figure 16. RDS Flowchart

4. Programming with Commands (Si4702/03 Rev C or Later Device Only)

The Si4702/03-C device provides additional functions and features that are not available in the Si4702/03-B16 device, while maintaining backward compatibility to the Si4702/03-B16 register set. In addition to the register-based programming method, the Si4702/03-C device may be programmed using commands, arguments, properties, and responses.

Commands control actions, such as set property value or get property value, and are one byte in size. Arguments are specific to a given command and are used to modify the command. For example, the PROPERTY_INDEX argument is required for the GET_PROPERTY command. Arguments are one byte in size, and each command may require up to seven arguments. Responses provide the system controller status information and returned after a command bits associated arguments are issued. Commands may return up to 7 additional response bytes. A complete list of commands is available in 5. "Command and Properties (Si4702/03 Rev C and Later Device Only)".

The command interface uses the RDSA, RDSB, RDSC and RDSD registers. In order to send commands RDS bit (Register 4, bit 12) must be disabled for the duration of the command processing by setting RDS = 0.

To send a command, write registers 0Ch–0Fh (RDSA–RDSD) with the desired arguments and command, then poll register 0Fh (RDSD) until the least significant byte is 0x00. At this point the response (if applicable) is available in registers 0Ch–0Fh (RDSA–RDSD).

There will be a delay between the time that RDS bit is set to 0 and a command may be sent. In order to determine when the command processor is enabled, write register 0Fh to 0x00FF and poll until register 0Fh is 0x0000.

Responses provide the user information and are echoed after a command and associated arguments are issued.

Table 17. Format for Programming with Commands (Si4702/03 Rev C or Later Device Only)

Register Name		Register Address	Command	
			High	Low
RDSA	**COMMAND1**	0Ch	ARG0	ARG1
RDSB	**COMMAND2**	0Dh	ARG2	ARG3
RDSC	**COMMAND3**	0Eh	ARG4	ARG5
RDSD	**COMMAND4**	0Fh	ARG6	CMD

Register Name		Register Address	Response	
			High	Low
RDSA	**RESPONSE1**	0Ch	RESP0	RESP1
RDSB	**RESPONSE2**	0Dh	RESP2	RESP3
RDSC	**RESPONSE3**	0Eh	RESP4	RESP5
RDSD	**RESPONSE4**	0Fh	RESP6	STATUS

4.1. Programming in Command in 2-wire Control Interface Mode

Table 18 demonstrates the command and response procedure implemented in the system controller to use the 2-wire bus mode. In this example the GET_PROPERTY command is demonstrated.

In 2-wire mode, care must be taken to write register 02h–0Bh with the original values since the RDSA–RDSD register are at the end of the 2-wire mode.

Table 18. Command and Response Procedure—2-Wire Bus Mode (Si4702/03 Rev C or Later Device Only)

	Action	Data	Description
REG 02h–0Bh	Write	0x--	Write with the original value.
ARG0	Write	0x00	
ARG1	Write	0x00	
ARG2	Write	0x00	
ARG3	Write	0x00	
ARG4	Write	0x03	PROPERTY_INDEX High Byte
ARG5	Write	0x01	PROPERTY_INDEX Low Byte
ARG6	Write	0x00	
CMD	Write	0x08	GET_PROPERTY for BLEND_STEREO_RSSI
REG 0Ah–0Bh	Read	0x--	Read starts from Register 0Ah.
RESP0–6	Read	0x--	Response data are only valid when STATUS is set to 0x00.
STATUS	Read	0x08	Reply Status. Response data are not valid.
REG 0Ah–0Bh	Read	0x--	Read starts from Register 0Ah.
RESP0–6	Read	0x--	Response data are only valid when STATUS is set to 0x00.
STATUS	Read	0x00	Reply Status. Response data are valid.

To send the GET_PROPERTY command and arguments, the system controller sends the START condition, followed by the 8-bit control word, which consists of the seven-bit address (00100000b) and the write bit (0b). The device acknowledges the control word by setting SDIO = 0, indicated by ACK = 0. The system controller then sends the REG 02h HI byte, and again the device acknowledges by setting ACK = 0. The system controller and device repeat this process for REG 02h LO, REG 03h HI–REG 0Bh LO, ARG0, ARG1, ARG2, ARG3, ARG4, ARG5, ARG6, and CMD byte. All seven arguments bytes must be sent for all commands, and unused arguments must be written 0x00.

START	ADDR + W	ACK	REG 02h HI	ACK	REG 02h LO	ACK	…	ACK	REG 11h LO	ACK	ARG0	ACK	…	ARG6	ACK	CMD	ACK	STOP
START	0x20	0	0x--	0	0x--	0	…	0	0x--	0	0x00	0	…	0x00	0	0x08	0	STOP

To read the status and response from the device, the system controller sends the START condition, followed by the eight-bit control word, which consists of seven bit device address and the read bit (1b). In this example, the write control word is ADDR+R = 00100001b = 0x21. The device acknowledges the control word by setting ACK = 0. Next the system controller reads the REG 0Ah HI byte. The system controller and device repeat this process for the REG 0Ah LO, REG 0Bh HI, REG 0Bh LO, RESP0, RESP1, RESP2, RESP3, RESP4, RESP5, RESP6, and STATUS bytes. In this example, STATUS byte is 0x08, indicating that the data are not ready. The response bytes are not valid and must be ignored. This process is repeated until the STATUS byte is set to 0x00.

START	ADDR + R	ACK	REG 0Ah HI	ACK	REG 0Ah LO	ACK	REG 0Bh HI	ACK	REG 0Bh LO	ACK	RESP0	ACK	…	RESP6	ACK	STATUS	ACK	STOP
START	0x21	0	0x--	0	0x--	0	0x--	0	0x00	0	0x--	0	…	0x--	0	0X08	0	STOP

When the STATUS byte returns 0x00, the system controller may use the response bytes from the device. However, unused response bytes return random data and must be ignored.

START	ADDR + R	ACK	REG 0Ah HI	ACK	REG 0Ah LO	ACK	REG 0Bh HI	ACK	REG 0Bh LO	ACK	RESP0	ACK	…	RESP6	ACK	STATUS	ACK	STOP
START	0x21	0	0x--	0	0x--	0	0x--	0	0x00	0	0x--	0	…	0x--	0	0X00	0	STOP

4.2. Programming in Command in 3-write Control Interface Mode

Table 19 demonstrates the command and respond procedure implemented in the system controller to use the 3-wire bus mode. In this example, GET_PROPERTY command is demonstrated. In 3-wire mode, register 0Fh must be the last register written.

Table 19. Command and Response Procedure—3-Wire Bus Mode (Si4702/03 Rev C or Later Device Only)

	Action	Data	Description
ARG0/1	Write	0x0000	
ARG2/3	Write	0x0000	
ARG4/5	Write	0x0301	PROPERTY_INDEX
ARG6/CMD	Write	0x0008	GET_PROPERTY for BLEND_STEREO_RSSI
RESP6/STATUS	Read	0x0008	Reply Status. Data is not ready.
RESP6/STATUS	Read	0x0000	Reply Status. Data is ready.

To send the GET_PROPERTY command and arguments, the system controller sets $\overline{SEN}$ = 0. Next, the controller drives the 9-bit control word on SDIO, consisting of the device address (A7:A5 = 101b), the write bit (0b), the device address (A4 = 0b), and register address for the COMMAND1 register (A3:A0 = 1100b). The control word is followed by a 16-bit data word, consisting of ARG0 followed by ARG1. The system controller then sets $\overline{SEN}$ = 1 and pulses SCLK high and then low one final time.

$\overline{SEN}$	Control	ARG0	ARG1	$\overline{SEN}$	SCLK
1 → 0	10101100b	0x00	0x00	0 → 1	Pulse

Next, the controller sends ARG2 and ARG3 of the command by driving drives the 9-bit control word on SDIO, consisting of the device address (A7:A5 = 101b), the write bit (0b), the device address (A4 = 0b), and register address for the COMMAND2 register (A3:A0 = 1101b). The control word is followed by a 16-bit data word, consisting of ARG2 followed by ARG3. The system controller then sets $\overline{SEN}$ = 1 and pulses SCLK high and then low one final time.

$\overline{SEN}$	Control	ARG2	ARG3	$\overline{SEN}$	SCLK
1 → 0	10101101b	0x00	0x00	0 → 1	Pulse

Next, the controller sends ARG4 and ARG5 of the command by driving drives the 9-bit control word on SDIO, consisting of the device address (A7:A5 = 101b), the write bit (0b), the device address (A4 = 0b), and register address for the COMMAND3 register (A3:A0 = 1110b). The control word is followed by a 16-bit data word, consisting of ARG4 followed by ARG5. The system controller then sets $\overline{SEN}$ = 1 and pulses SCLK high and then low one final time.

$\overline{SEN}$	Control	ARG4	ARG5	$\overline{SEN}$	SCLK
1 → 0	10101110b	0x03	0x00	0 → 1	Pulse

Next, the controller sends ARG6 and CMD of the command by driving drives the 9-bit control word on SDIO, consisting of the device address (A7:A5 = 101b), the write bit (0b), the device address (A4 = 0b), and register address for the COMMAND4 register (A3:A0 = 1111b). The control word is followed by a 16-bit data word, consisting of ARG6 followed by CMD. The system controller then sets $\overline{SEN}$ = 1 and pulses SCLK high and then low one final time.

$\overline{SEN}$	Control	ARG6	CMD	$\overline{SEN}$	SCLK
1 → 0	10101111b	0x00	0x08	0 → 1	Pulse

To read the status and response from the device, the system controller sets $\overline{SEN}$ = 0. Next, the controller drives the 9-bit control word on SDIO, consisting of the device address (A7:A5 = 101b), the read bit (1b), the device address (A4 = 0b), and register address for the RESPONSE4 register (A3:A0 = 1111b). The control word is followed by a 16-bit data word, consisting of RESP6 followed by STATUS. The system controller then sets $\overline{SEN}$ = 1 and pulses SCLK high and then low one final time. In this example, the STATUS byte is 0x08, indicating that the response data are not ready. The device is not ready to accept another command. RESP6 is random until the STATUS byte is 0x00. This process should be repeated until the STATUS byte is set to 0x00.

$\overline{SEN}$	Control	RESP7	STATUS	$\overline{SEN}$	SCLK
1 → 0	10111111b	0x00	0x08	0 → 1	Pulse

When the STATUS byte is set to 0x00, the system controller may read the response bytes from the device in any order.

$\overline{SEN}$	Control	RESP7	STATUS	$\overline{SEN}$	SCLK
1 → 0	10111111b	0x00	0x00	0 → 1	Pulse

If the reply included RESP0 and RESP1 bytes, the system controller sets $\overline{SEN}$ = 0, and then the controller drives the 9-bit control word on SDIO, consisting of the device address (A7:A5 = 101b), the read bit (1b), the device address (A4 = 0b), and register address for the RESPONSE1 register (A3:A0 = 1100b). The control word is followed by a 16-bit data word, consisting of RESP0 followed by RESP1. The system controller then sets $\overline{SEN}$ = 1 and pulses SCLK high and then low one final time.

$\overline{SEN}$	Control	RESP0	RESP1	$\overline{SEN}$	SCLK
1 → 0	10111101b	0x--	0x--	0 → 1	Pulse

5. Command and Properties (Si4702/03 Rev C and Later Device Only)

Table 20. Si4702/03 Command Summary (Si4702/03 Rev C or Later Device Only)

CMD	Name	Description
0x07	SET_PROPERTY	Sets the value of a property.
0x08	GET_PROPERTY	Retrieves a property's value.
0xFF	VERIFY_COMMAND	This command can be used to determine that the command processor is enabled.

5.1. Si4702/03 Commands (Si4702/03 Rev C or Later Device Only)

Command 0x07 SET PROPERTY

Sets a property shown in Section 5.2. "Si4702/03 Properties (Si4702/03 Rev C or Later Device Only)". This command may only be sent when in powerup mode.

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**
ARG0	PROPERTY_VALUE[15:8]							
ARG1	PROPERTY_VALUE[7:0]							
ARG2	Always write to 0							
ARG3	Always write to 0							
ARG4	PROPERTY_INDEX[15:8]							
ARG5	PROPERTY_INDEX[7:0]							
ARG6	Always write to 0							

Command 0x08 GET PROPERTY

Gets a property shown in Section 5.2. This command may only be sent when in powerup mode.

Response bytes: Two

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	0	0	0	0	1	0	0	0
ARG0	Always write to 0							
ARG1	Always write to 0							
ARG2	Always write to 0							
ARG3	Always write to 0							
ARG4	PROPERTY_INDEX[15:8]							
ARG5	PROPERTY_INDEX[7:0]							
ARG6	Always write to 0							

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
RESP0	PROPERTY VALUE [15:8]							
RESP1	PROPERTY VALUE [7:0]							

Command 0xFF VERIFY_COMMAND

This command can be used to determine that the command processor is enabled. Send this command and poll to see that the command byte has been cleared.

Response bytes: None

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	1	1	1	1	1	1	1	1
ARG0	Always write to 0							
ARG1	Always write to 0							
ARG2	Always write to 0							
ARG3	Always write to 0							
ARG4	Always write to 0							
ARG5	Always write to 0							
ARG6	Always write to 0							

5.2. Si4702/03 Properties (Si4702/03 Rev C or Later Device Only)

Property 0x0200. FM_DETECTOR_SNR (Default 0)

Selects the SNR where the FM detector switches modes. Default of 0 is backward compatible with Si4702/03-B16 FM detector.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	FDSNR[7:0]							

Bit	Name	Function
D15:D8	Reserved	Always write to 0.
D7:D0	FDSNR	Sets threshold for FM detector.

SNR >12 → differential detector

12 > SNR > threshold → impulse reject detector

threshold > SNR > 0 → slew rate detector

Property 0x0300 BLEND_MONO_RSSI (Default 31)

Sets the RSSI level to enable full mono audio output. At RSSI levels more than BLEND_MONO_RSSI, but less than BLEND_STEREO_RSSI, stereo separation will be reduced. If this property is used, it is recommended that the BLENDADJ bits be set to 0.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	BMR[7:0]							

Bit	Name	Function
D15:D8	Reserved	Always write to 0.
D7:D0	BMR	Sets threshold for full mono audio output.

Property 0x0301 BLEND_STEREO_RSSI (Default 50)

Sets the RSSI level to enable full stereo audio output. At RSSI levels more than BLEND_MONO_RSSI, but less than BLEND_STEREO_RSSI, stereo separation will be reduced. If this property is used, it is recommended that the BLENDADJ bits be set to 0.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	BSR[7:0]							

Bit	Name	Function
D15:D8	Reserved	Always write to 0.
D7:D0	BSR	Sets threshold for full stereo audio output.

Property 0x0700 CALCODE (Default n/a) READ-ONLY

Internal calibration result of the powerup sequence. This result may be used to troubleshoot crystal oscillator/RCLK operation. See 2.1.1. "Hardware Initialization" step 5.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	CALCODE[15:0]															

Bit	Name	Function
D15:D0	CALCODE	Internal calibration result of the powerup sequence.

Property 0x0C00 SNRDB (Default n/a) READ-ONLY

SNR level (in 2 dB steps) that the seek algorithm is seeing. FM_DETECTOR_SNR uses this value to compare to the threshold.

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	0	0	0	0	0	0	0	0	SNRDB[7:0]							

Bit	Name	Function
D15:D8	Reserved	Always write to 0.
D7:D0	SNRDB	SNR level (in 2 dB steps) that the seek algorithm is compared to.

APPENDIX—SEEK ADJUSTABILITY AND SETTINGS

Introduction

An important feature of an FM radio receiver is its ability to reliably identify valid stations during a seek operation. This feature allows end customers to seek from one valid station to the next up and down the FM band. It also allows manufacturers to create host software to automatically populate a list of valid stations in a given area. However, reliably identifying and separating valid stations from noise or poor-quality stations is challenging in any environment, especially portable devices. The Silicon Laboratories Si4700/01/02/03 FM Tuner family provides a highly reliable seek algorithm, and also adds adjustability so that manufacturers and/or end users can customize seek settings to accommodate individual tastes or changing RF environments.

Default Seek Qualifiers

The most commonly used measurement of valid stations is the total received power at a given channel compared to a threshold. In the Si4700/01/02/03 family, this power measurement is Received Signal Strength Indicator (RSSI), measured as the integrated power after the channel filter for a given channel. The RSSI seek threshold (SEEKTH) is simply the power level above which a valid channel is determined. Setting the seek threshold too high may result in missed valid channels; too low may result in false detections.

To augment the accuracy of this metric, the Si4700/01/02/03 incorporates a second indicator of valid channels called Automatic Frequency Control Rail, or AFC rail. AFC rail is used to detect the condition wherein an adjacent channel's power is detected at the tuned frequency, potentially detecting a false positive. If a tuned channel's RSSI is above the seek threshold, but the AFC has tracked from the center of the channel by a given number of kHz, the channel can reliably be determined to be an invalid station.

Using the RSSI threshold in conjunction with AFC rail offers seek performance with a greater than 90% probability of finding only valid stations and a sub-4 second scan time for auto-populating valid stations.

Note: Figures given represent a competitive host micro-controller, 200 kHz channel spacing, and 87.5–108 MHz band setting.

Advanced Seek Offerings

FM environments typically generate a shaped noise profile, making it almost impossible to set a seek threshold which is both above the noise floor and within valid station levels. The noise floor can vary due to many factors including antenna impedance and matching, signal environment, AGC setting, and noise sources. In particular, office and lab environments have elevated noise levels across the FM band due to the presence of electronic and computer equipment. An example RSSI spectrum is shown below in Figure 17. Note that valid stations are indicated by their frequencies.

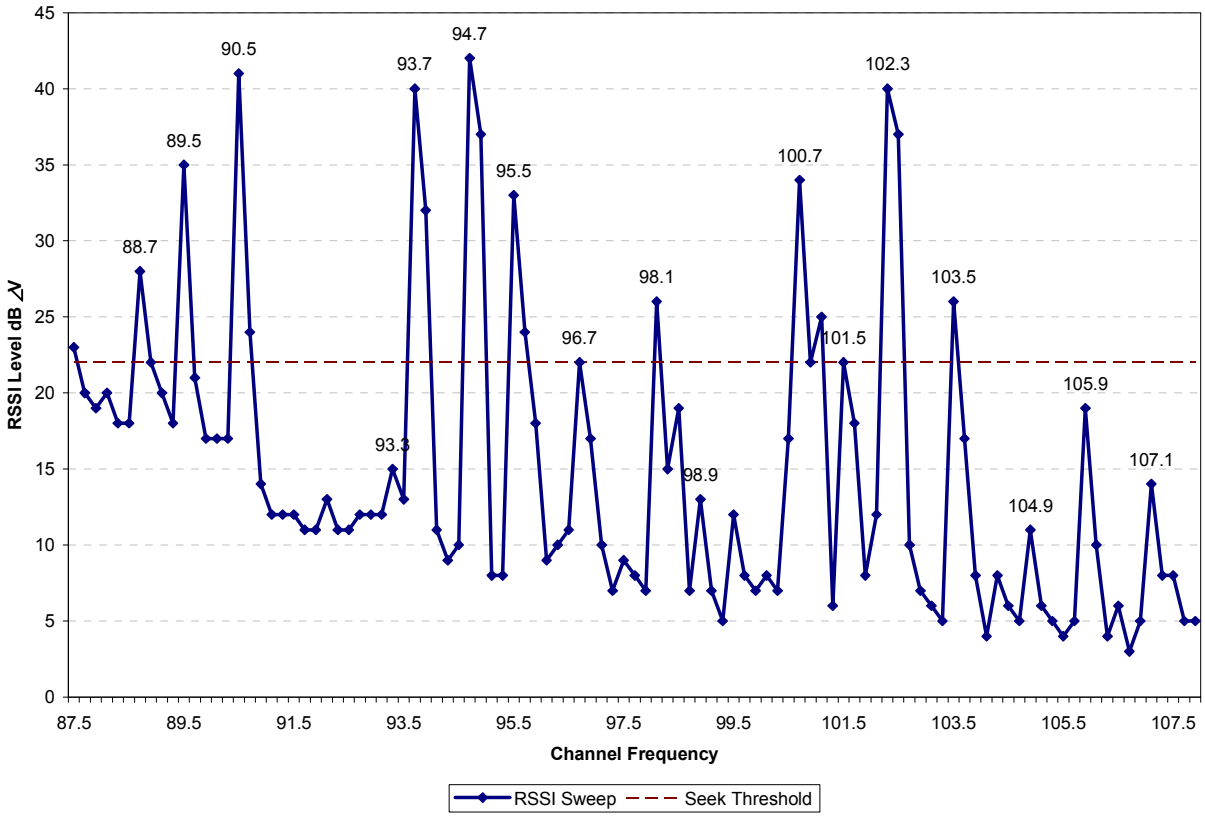


Figure 17. Sample RSSI Spectrum

In Figure 17, the valid stations at 93.3, 98.9, 104.9, 105.9, and 107.1 are difficult to detect since their RSSI levels are below the noise level of the spectrum at some unpopulated channels. Setting the RSSI seek threshold to a value of 12 would likely detect these valid stations, but could have false positives at many invalid channels. Setting the seek threshold to 22 as shown avoids false detections but could miss these valid stations.

The Si4700/01/02/03 devices incorporate additional valid station qualifiers to more reliably detect lower RSSI stations and screen out invalid stations. These qualifiers are optional and adjustable so that customers and end users may adjust seek as desired.

The additional qualifiers run sequentially to the first two tests discussed above. The first qualifier, SNR, compares a tuned channel's SNR to an SNR threshold. The SNR threshold is adjustable in SKSNR[3:0]. Example SKSNR[3:0] threshold values and likely results are shown in Table 21.

Table 21. Sample SKSNR[3:0] Settings

SKSNR[3:0] Write Value	Desired SNR Threshold	Seek Result Relative to Default Seek Metrics
0x0	Disabled	NA
0x4	Good SNR threshold	Increased reliability, only good stations qualified
0x7	Better SNR threshold	Increased reliability, only better stations qualified

The second qualifier in Si4700/01/02/03 devices measures the number of FM impulses detected at a tuned channel. FM Impulse noise occurs in all FM detectors when the SNR of a received station becomes very low and the received noise causes the FM detector to make instantaneous phase jumps, resulting in audible "clicks." For a noisy signal, more FM impulses are typically received, and conversely for a higher quality signal, fewer or no FM impulses are received. The Si4700/01/02/03 detects these FM impulses and applies a smoothing filter to minimize their impact on sound quality. FM impulses can also be used as a metric to determine the quality of the audio present on a given channel. This qualifier is optional and adjustable.

The SKCNT register sets a threshold for the number of FM impulses allowed on a tuned channel within a defined period.

Note: The period and algorithm for measuring FM impulses is proprietary to Silicon Laboratories, Inc. and will not be explained further.

Table 22 provides some example settings and approximate results.

Table 22. Sample SKCNT[3:0] Settings

SKCNT[3:0] Write Value	Desired Impulse Threshold	Seek Result Relative to Default Seek Metrics + SNR Threshold
0x0	Disabled	NA
0x8	Allows more FM impulses	Increased reliability, more stringent valid station requirements
0xF	Allows fewer FM impulses	Highest reliability, most stringent valid station requirements

Note: By increasing the stringency of SKSNR and SKCNT settings, stations that have low SNR or high levels of FM impulse noise may be rejected. Typically, these stations do not have good audio quality and customers do not wish to listen to them; however, if customers are specifically searching for these stations, be aware that a stringent seek algorithm may disqualify them as valid stations.

Seek Algorithm Sequencing

The seek algorithm sequencing is shown in the flowchart in Figure 18.

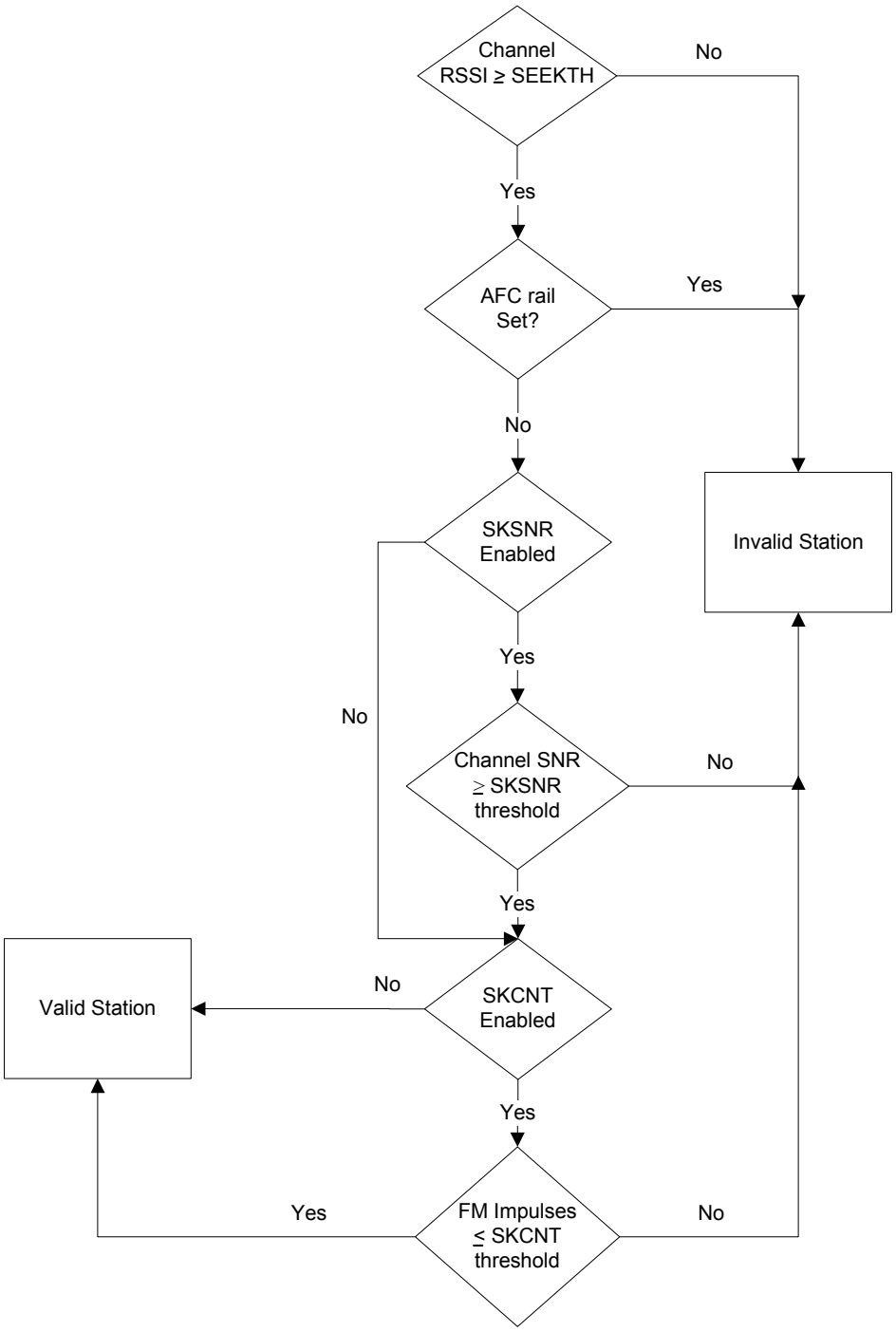


Figure 18. Seek Algorithm Flowchart

Note: Both SNR and FM impulse count are independent and can be run as additional qualifiers with or without the other.

Seek Results Comparisons

Figure 19 compares Silicon Laboratories field trials with existing and new seek parameters. The graph illustrates that by setting the RSSI seek threshold at 25, invalid channels are not detected; however several valid stations are missed. Conversely, with the RSSI threshold at 12, several invalid stations are identified. With the new optional qualifiers enabled with the RSSI threshold at 12, the invalid stations are rejected and valid stations are reliably identified.

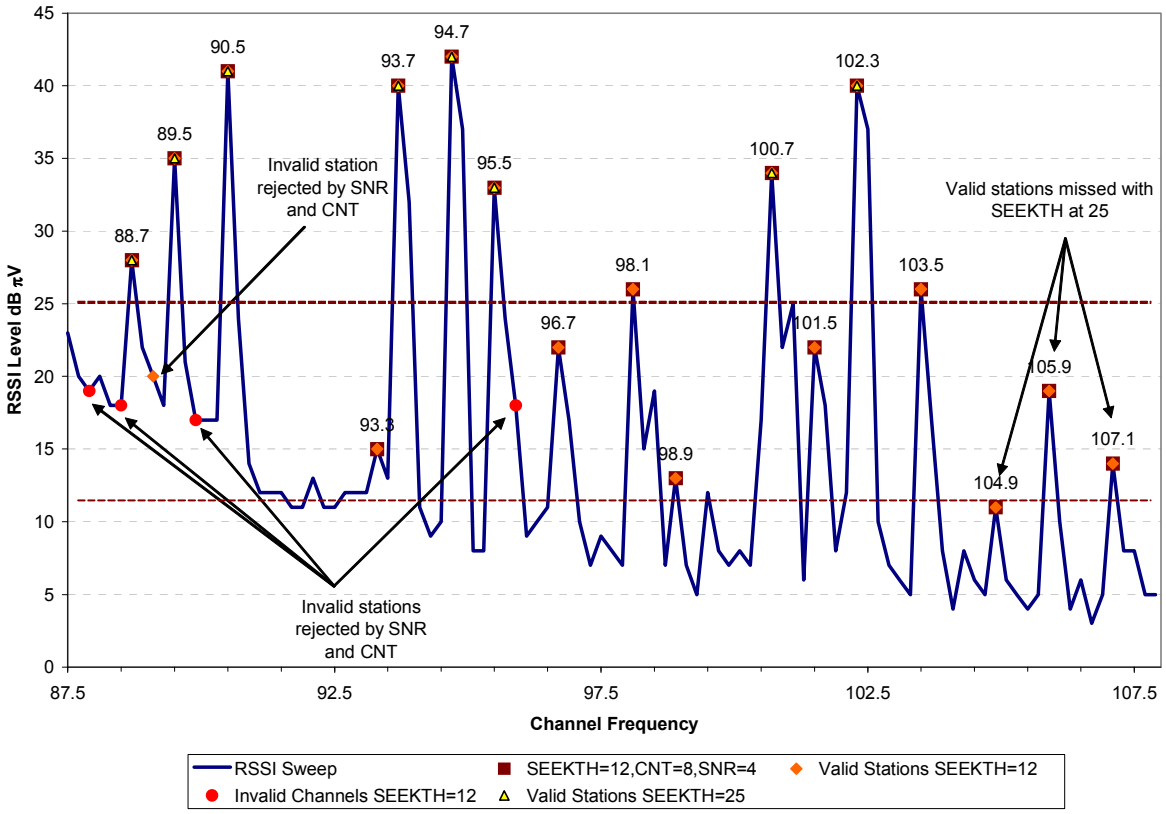


Figure 19. Seek Results Comparison

Seek Settings Recommendations

Table 23 summarizes the seek settings discussed above. These settings are adjustable to address customers' system design, target markets, and subjective preferences and have been found to yield good performance in most applications.

Table 23. Summary of Seek Settings

Configuration	Comments	SEEKTH[7:0]	SKSNR[3:0]	SKCNT[3:0]
Default	Compatible with Firmware 14	0x19	0x0 (disabled)	0x0 (disabled)
Recommended	Relative to Firmware 14	0x19 (typical)	0x4—Good SNR	0x8—Fewer FM impulses
More Stations	Reduced SEEKTH identifies valid stations in low RSSI environments	0xC (typical)	0x4—Good SNR	0x8—Fewer FM impulses
Good Quality Stations Only	Identifies only good quality stations	0xC	0x7—Better SNR	0xF—Fewest FM impulses
Most Stations	Seek algorithm relies solely on AFC rail, SNR and FM impulse; Most valid stations identified; Potential for slightly longer seek time	0x0	0x4—Good SNR	0xF—Fewest FM impulses

DOCUMENT CHANGE LIST

Revision 0.42 to Revision 0.43

- Added Sections 4. "Programming with Commands (Si4702/03 Rev C or Later Device Only)" and 5. "Command and Properties (Si4702/03 Rev C and Later Device Only)".

Revision 0.43 to Revision 0.44

- Updated "4.1.Programming in Command in 2-wire Control Interface Mode" on page 27.
- Updated command register "Property 0x0200. FM_DETECTOR_SNR (Default 0)" on page 33.

Revision 0.44 to Revision 0.5

- Added Si4703-C19 Errata description:
  - Updated 2.1.1 Hardware Initialization.
  - Updated 2.1.2 Hardware Powerdown.
  - Updated Figure 2 on page 6.

Revision 0.5 to Revision 0.6

- Added "Appendix—Seek Adjustability and Settings".
- Expanded Sections 3.3.4–3.3.6
- Added description of setting GPIO1/2/3 low to Table 4.
- Clarified Section 3.2.1 and Table 3.
- Removed NDA.

Revision 0.6 to Revision 0.61

- Added 0.5 to 0.6 revision list.

Revision 0.61 to Revision 0.62

- Updated Table 20, "Si4702/03 Command Summary (Si4702/03 Rev C or Later Device Only)," on page 30.

Revision 0.62 to Revision 0.7

- Updated Table 21, "Sample SKSNR[3:0] Settings," on page 37 and Table 23, "Summary of Seek Settings," on page 40.

Revision 0.7 to Revision 0.8

- Updated BLEND_MONO_RSSI, BLEND_STEREO_RSSI property index in Tables 18, 19, and Section 5.2.

Revision 0.8 to Revision 0.9

- Updated "2.1.1.Hardware Initialization" on page 5 step 5.
- Updated Register , "Property 0x0C00 SNRDB (Default n/a) READ-ONLY," on page 34.

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